PENDING CLAIMS

1. (Amended) A method for processing software instructions comprising,

decomposing a macroinstruction into a plurality of microinstructions,

issuing all of the plurality of microinstructions simultaneously, in parallel,

executing all of the plurality of microinstructions simultaneously, in lockstep,

determining whether an exception occurs in any of the microinstructions, and

if an exception occurs in any of the microinstructions, canceling all of the microinstructions.

3. (Amended) The method of claim 1, wherein the microinstructions are executed on separate execution units, but appear as though they were executed on a single execution unit.

4. (Amended) The method of claim 1, wherein all of the microinstructions are executed on the same clock cycle.

5. (Amended) The method of claim 1, wherein the microinstructions are executed over multiple clock cycles.

6. The method of claim 1, wherein the method is implemented in a system emulating SSE instructions.

7. The method of claim 6, wherein the system allows a single instruction to operate on multiple single-precision ("SP") floating-point ("FP") values.

8. (Amended) The method of claim 1, further comprising updating a flag based upon a result of the execution of the microinstructions.

9. (Amended) The method of claim 1, further comprising,

if an unmasked exception occurs, canceling the execution of all of the plurality of microinstructions, without regard to the relative ages of each of the plurality of microinstructions, and invoking a microcode handler, and

if an unmasked exception does not occur, updating at least one exception flag by independently generating a logical OR of exceptions for a plurality of functional units.

10. A method for processing software instructions comprising,

(a) providing two microinstructions to emulate a high-half and a low-half SSE operation,

(b) forcing the high-half and low-half operations to issue in parallel,

(c) dispatching the high-half and low-half operations simultaneously to a first FP unit and to a second FP unit, respectively,

(d) generating a signal from an emulator's hardware,

(e) sending the signal to the first and second FP functional units,

(f) determining whether an exception is taken in either the first or the second FP unit,

(g) if an exception is taken in either the first or second FP unit, flushing a result in the other FP unit, and

(h) updating MXCSR flags based upon the results of the first and second FP units.

11. The method of claim 10, wherein the flushing of a result in the other FP unit does not depend upon the relative ages of the two microinstructions.

12. (Amended) A computer system comprising,

a processor comprising,

(a) a floating point unit;

(b) a ROM;

(c) a plurality of floating point registers;

wherein the processor is configured to emulate an instruction set by:

(a) decomposing a macroinstruction into a plurality of microinstructions;

(b) issuing all of the plurality of microinstructions simultaneously, in parallel,

(c) determining whether an exception occurs in any of the microinstructions, and

(d) if an exception occurs in any of the microinstructions, canceling all of the microinstructions.

13. (Amended) The computer system of claim 12, wherein the processor is further configured to emulate the instruction set by executing all of the microinstructions.

14. (Amended) The computer system of claim 13, wherein the microinstructions are executed on separate execution units, but appear as though they were executed on a single execution unit.

15. (Amended) The computer system of claim 14, wherein the processor is further configured to emulate an instruction set by updating a flag based upon a result of the execution of the microinstructions.

16. (Amended) The computer system of claim 15, wherein the processor is further configured to emulate an instruction set by

determining whether an exception occurs in the execution of any of the microinstructions,

if an exception occurs, causing the exception to cancel all of the microinstructions.

17. The computer system of claim 12, wherein the instruction set is a SSE instruction set.

18. The computer system of claim 17, further comprising an FP register having 82 bits, wherein the computer system uses two FP registers to emulate four 32-bit single-precision, floating point values in an SSE register.

19. The method of claim 1, wherein the step of issuing comprises forcing the microinstructions to issue simultaneously, in lockstep with each other, and wherein the step of canceling comprises canceling all of the plurality of microinstructions without regard to the relative ages of the microinstructions and without using a backoff mechanism.

20. The method of claim 10, wherein the step of forcing the high-half and low-half operations to issue in parallel comprises causing the high-half and low-half operations to execute simultaneously in lockstep with each other, and wherein the step of flushing a result comprises canceling each of the high-half and low-half operations if an exception is taken in either the first or second FP unit.